IN THE SPECIFICATION:

Please replace paragraph number **[0004]** with the following rewritten paragraph:

[0004] Accordingly, there has been a need to form a fine-pitched electrically conductive coupling mechanism for coupling with the fine-pitched contact or bond pads of integrated circuits located across a semiconductor substrate. Formation of an intermediary coupling mechanism such as a contactor card for locating between a semiconductor substrate (e.g., a wafer-under-test) and a probe card of a testing system has been attempted. The contactor card by necessity needs to electrically couple signals from its first side to its second or opposing side. While the electrical signals can be routed on either side to a ~~non-~~nondirectly opposing arrangement, the signals must be necessarily routed from one side or face through the entire contactor card to a second or opposing face. One conventional approach for electrically coupling a signal from a first side of a wafer-scale contactor card to a second side involved the formation of a physical hole entirely through the thickness dimension of the contactor card. To facilitate electrical conduction through the physical hole, conductive (solder) paste was screened into the hole. Because of the imprecise application process and inconsistency of the conductive paste through the hole, gases and solvents easily become trapped and isolated within the conductive paste-based contact.

Please replace paragraph number **[0020]** with the following rewritten paragraph:

[0020] FIG. 1 illustrates a cross-sectional view of a semiconductor wafer or substrate ~~12~~ 12, within which it is desirable to form or pass a connection ~~through~~ through, ~~the entire substrate~~ from a first side 14 to a second side 16. Substrate 12 may be implemented as a semiconductor substrate such as a silicon wafer and may include varying diameters such as 4 inch, 6 inch, 8 inch and 12 inch or larger wafers. While various sizes of semiconductor wafers are described herein, the various embodiments of the present invention find application in various substrate environments where an electrical connection structure between a first side to a second side thereof is desirable. With regard to typical thicknesses, a typical 4 inch wafer, for

example, may have a thickness, for example, of approximately 500 microns while an 8 inch diameter wafer, for example, may include a thickness of approximately 725 microns. Furthermore, the composition of substrate 12 may further include other semiconductive compositions such as gallium arsenide or indium phosphide and may further include ~~non-~~nonconductive or insulative compositions, such as glass, as a suitable substrate 12. Furthermore, first and second sides 14 and 16 may further include conductive traces as described below with reference to FIG. 9. Additionally, first and/or second sides 14 and 16 may further include circuits or other functionality which may benefit from the formation of an electrically conductive connection between first side 14 and second side 16 of semiconductor substrate 12.

Please replace paragraph number **[0021]** with the following rewritten paragraph:

[0021] FIG. 1 further illustrates the formation of a hole 10 which may comprise one or more profiles formed from the removal of substrate material between a first side 14 and a second side 16. Hole 10, for example, may ~~be of~~ be less than 100 microns in diameter, and 50 micron diameter through-holes have become conventional. It is contemplated that in the near future 30 micron diameter through-holes may be commonplace. Removal of such material may take place through the use of a device 18 which may include a mechanical means, such as a mechanical drill, or an electromagnetic device, such as a laser for ablating substrate material. By way of example and not limitation, device 18 may include a laser, an example of which is a 7 watt, 355 nanometer wavelength laser available from Xsil, Ltd. of Dublin, Ireland. The hole 10 through substrate 12 may be further formed by way of a chemical etching process, such as a plasma etching process. An exemplary etch process for use with the silicon substrate may also include a SF_6 or other etching process, the specifics of which are appreciated by those of ordinary skill in the art and are not further described herein. As described above, other substrate compositions may be utilized which would require a corresponding etch process for the formation of hole 10 within substrate 12.

Please replace paragraph number **[0026]** with the following rewritten paragraph:

[0026] By coating the seed layer 27 with the conductive plating 36 of a suitable metal, an annular conductive path is created through the hole 20 (FIG. 2). The electroless plating process forms a substantially conformal coating in the hole 20 that is substantially free of any voids or keyholes. The conductive layer ~~130~~ formed from the electroless plating process will typically have a uniform thickness, a low porosity, will provide corrosion protection and will be relatively hard. The electroless plating process is accomplished by placing the substrate 12 into a bath containing an aqueous solution of the metal to be deposited in ionic form. The aqueous solution also includes a chemical reducing agent such that the metal may be deposited without the use of electrical energy. The driving force for the reduction of the metal ions and subsequent deposition in the electroless plating process is driven by the chemical reducing agent. The reduction reaction is essentially constant at all points on the seed layer 27 so long as the aqueous solution is sufficiently agitated by pressurized flow to ensure that a uniform concentration of metal ions and reducing agents are distributed in the aqueous solution.

Please replace paragraph number **[0027]** with the following rewritten paragraph:

[0027] FIG. 2 illustrates a through-hole conductor formed in accordance with an embodiment of the present invention. A through-hole conductor 30 is formed between first and second sides 14 and 16 through substrate 12 by forcing the plating solution (not shown) from a high-pressure side of substrate 12 in a flow direction 32 to a low-pressure side thereof. Due to the passage of plating solution in this directed flow process, conductive plating 36 forms on inner surface 26 in a generally uniform manner. Due to the pressurized flow of the plating solution, substantially uniform plating results when fresh plating solution having a generally uniform concentration passes through the physical hole 10 within substrate 12 followed by the periodic cycling of power in the electroplating process. The cycling of the power is timed and sequenced to allow fresh fluid or uniform concentrated fluid to pass into the hole prior to the reactivation of the electroplating power. Electroplating may be preceded by an electroless, or immersion plating process to deposit, ~~gold~~ gold, nickel or other suitable metal layer on the sidewalls of hole 20 to

facilitate the electroplating. It is appreciated that at some point in time in such a continuous process, the formation of conductive plating 36 may build up and result in a physical barrier between the high-pressure side and the low-pressure side thereby restricting the flow of plating solution therebetween.

Please replace paragraph number **[0031]** with the following rewritten paragraph:

[0031] FIG. 4 illustrates a single wafer plating system for forming through-hole conductors, in accordance with an embodiment of the present invention. A single wafer plating system 50 includes a plating tank 52 configured for placing therein a semiconductor wafer 68 which, in one embodiment, may be loaded into a plating fixture 66 to form a loaded fixture 64. As shown, loaded fixture 64 may be simply retained across the width of the plating tank 52 by retention slots or other fixturing. As described above, a barrier is formed between a high-pressure side 54 and a low-pressure side 56 of tank 52 which induces a flow direction 58 of a plating solution from a high-pressure bath 60 to a low-pressure bath ~~64~~ 62. By way of example and not limitation, plating solutions within the respective baths may include copper sulphate or nickel sulphate if the conductive plating 36 (FIG. 2) is copper or nickel, respectively. Other plating chemistries, as appreciated by those of ordinary skill in the art, may also be employed to plate other metals such as, for example, silver and gold.

Please replace paragraph number **[0034]** with the following rewritten paragraph:

[0034] FIG. 6 illustrates a wafer electroplating system 100, in accordance with an embodiment of the present invention. An electroplating system 100 includes a plating tank 102 with one or more loaded fixtures 114, each including a semiconductor wafer or substrate 118 and a plating fixture 116. Electroplating system 100 is electrically configured with an electroplating power arrangement 120 comprised of a signal generator 122 for executing a specific electrical activation duty cycle as exhibited between electrodes 124 and 126. The electrode 124 may comprise a cathode operably coupled to a semiconductor wafer or substrate and an electrode 126 such as an anode. The plating solution flow direction 108 is maintained between a high-pressure

side 104 with a bath 110 to a low-pressure side 106 with a bath 112, each comprised ~~of~~ of a plating solution. The electroplating configuration may be further extended to a multiwafer arrangement as illustrated in FIG. 5.

Please replace paragraph number **[0036]** with the following rewritten paragraph:

[0036] FIG. 7 illustrates a cross-sectional view of a through-hole conductor formed in accordance with an embodiment of the present invention. The through-hole conductor and related processes described herein may further incorporate additional profiles which may further provide beneficial features. As illustrated, a through-hole conductor 130 including a conductive element 134 provides electrical conductivity through a semiconductor substrate 132 and may be electrically isolated from the semiconductor substrate 132 by ~~a~~ an insulator material layer 128, an example of which is described above as TEOS. Extended coupling profiles for physically coupling to an electrical connection through the semiconductor substrate 132 may be further accommodated by the addition of one or more conductive caps 136, 138 which extend the profile of the through-hole conductor 130 above the corresponding surface of the semiconductor substrate 132. Conductive caps 136, 138 may be formed on the ends of conductive element 134 by electroplating as known to those of ordinary skill in the art and are, therefore, not further described herein. Furthermore, a nickel/gold cap is also suitable for use as a contact.